Celerint is leading the way to eliminate index time from semiconductor test. We help our customers reach that goal today by providing licensed software control systems and proprietary hardware interfaces that leverage existing capital equipment and test programs to create an indexless test cell. The platform has met the manufacturing acceptance criteria at one of the world's leading semiconductor companies, and registered customers can preview their results using our proprietary Sentinel Controller™ Simulator.
DESCRIPTION

Legacy Equipment
Reconfigure your legacy ATE to eliminate its number one source of test inefficiency: index time. By multiplexing two handlers to a single tester, the increase in test cell throughput can be dramatic: up to twice the throughput. Even when factoring in the additional cost and floor space required for a second handler, the cost of test is often less than any competing alternative available on the market today. Celerint makes it easy by providing the control software and interface hardware to make it happen.

Celerint Licensed Control Software
Celerint offers control software for indexless test. The software has been fully qualified and is available in both native and PXI stand-alone versions for rapid deployment. The control software ensures reliable and high performance operation of the test cell under heavy production work loads.

- Coordination between tester and handler operations
- Control of multiplexing interface hardware
- Handler identification during STDF data log writes
- Monitoring of throughput and yield alarms and warnings
- Email and text notification of alarm events with optional data-log attachment
- Continued test cell operation even when one handler is offline

Celerint Multiplexing Interface
Celerint has invested significant time and resources developing multiplexing strategies that cover the full spectrum of test head resources. Whether it is complex mixed-signal test systems or high pin count digital systems, we have a solution.

- Semi-custom multiplexing test board
- XLNT5001 196 channel, high density, multiplexing module
- XLNT5068 multiplexing module test fixture
- Proprietary high performance soft-dock, HPSD™
- Soft-dock calibration fixtures
PLANNING AND CONFIGURING A SYSTEM

Planning Tools
Celerint provides tools that predict the financial and operational benefits of the tandem handler test cell. These are available at no cost to registered visitors on the Celerint website at http://www.celerint.com.

- Sentinel Controller Simulator™ (per unit cost and throughput per unit area of floor space)
- Cost of Test Spreadsheets (comprehensive cost of test scenario comparisons)
- SPICE models of multiplexed signal path
- Tandem handler test cell emulation: in a conference room or on the test floor using customer’s ATE

Test Program Changes
No change to the test program is required unless the customer requests traceability to handler ID during STDF data logging. In this case, a very minor change to the handler interface code is required. No changes to the test portion of the code is ever required.

Time To Implementation
Typically, the time to implementation is the time required to spin the multiplexing interface board for the first test head configuration. As the board design is test head specific, one board design works across all testers with equivalent or subset configurations.

Celerint Deliverables

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<td>XLNT5001 based design</td>
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Costs
Customers can expect a one time NRE for interface hardware, a software licensing fee, and flexible support options. Hardware is warrantied for one year, and software comes with free update support. Please contact a Celerint sales representative for a quote.